**AMENDMENTS TO THE SPECIFICATION**

Please replace the paragraph [006] on page 3 with the following amended paragraph.

BRIEF DESCRIPTION OF THE DRAWINGS

[006] The drawings refer to the invention in which:

figure 1 illustrates a diagram of a prior art output buffer with pre-driver circuits;

figure 2 illustrates a block diagram of an output buffer having capacitivly coupled feedback from the final output stage to the pull-up and pull-down pre-drivers;

figure 3 illustrates a simplified schematic diagram of an embodiment the pull-down portion of an output buffer having slew rate control circuitry;

figure 4 illustrates an embodiment of a transistor level schematic diagram of another pull-down portion of an output buffer having slew rate control circuitry~~the circuit shown in figure 3~~;

figure 5 illustrates an embodiment of a cross-sectional view of a folded capacitor; and

figure 6 illustrates an embodiment of schematic of a slew rate output buffer consisting of both the pull-up and pull-down drivers.

Please replace the paragraph [0022] on page 9 with the following amended paragraph.

[0022] Figure 4 is an embodiment of a transistor level schematic diagram of another pull-down portion of an output buffer having slew rate control circuitry.~~the circuit shown in figure 3.~~ Referring to figure 4, FET refers to a field effect transistor. NFET and

PFET refer respectively to an n- channel FET and a p-channel FET both of which are voltage controlled devices. FETs are also referred to as MOS devices or MOSFETs.

Please replace paragraph [0011] on page 5 with the following amended paragraph.

[0011] These components work together to force a controlled linear ramp on the buffer's output pad **302**. Amplifier **306** feedback capacitor **308**, and current mirror **314** together control the fall time of output pad **302** through pull-down transistor **304**. For example, if the buffer circuit **300** connects to a bus, then the amplifier **306**, feedback capacitor **308,** and current mirror **314** determine just how the bus transitions voltage from a high voltage state to a low voltage state. A voltage reference is established at approximately VREF. VREF is chosen for the convenience of the particular embodiment. The node SUM is held close to the voltage reference at all times by bias circuits (not shown in figure 3). The feedback current through feedback capacitor **308** on amplifier **306** acts to keep the sum terminal (SUM) close to the voltage reference. If the voltage value of SUM is above VREF, then the amplifier drives the gate **316** of pull-down transistor **304** higher. Conversely, if voltage value of SUM is lower than VREF, amplifier **306** drives the voltage on the gate **316** lower. The higher the voltage potential on the gate **316** increases the current from PAD 302 through driver transistor 304 to ground. This increases the magnitude of the edge rate on PAD 302. In an embodiment, the gate acts as the input terminal for driver amplifier referred to as pull-down transistor **304**.

Please replace paragraph [0023] on page 9 with the following amended paragraph.

[0023] PFET **410** maybe a current source for $i_{SRC.}$ controlled by voltage PBIAS1. PFET **410** sources for example, two units of current. The amplifier is a modified, folded cascode amplifier made up of NFETs **420**, **418** and PFETs **412**, **422**. NFET **420** and PFET **412** are a current steering pair, NFETs **416**, **418** make up the current sink for the amplifier. NFET **418** is controlled by voltage signal NBIAS1, and in this illustrative example, it sinks one unit of current. NFET 416 may act as a cascode for NFET 418. In an embodiment, having a positive current source and a negative current sink make the transition rate more linear throughout the entire transition range and reduces noise effects. In an embodiment, other types of current sources, with other current source or sink values or ratios, may be used as may be desired in other embodiments. The greater nominal levels of current flow minimize noise current effects and biasing the amplifier to constantly conduct allows the amplifier to operate in a linear range. NFET **416** acts as a cascode transistor to increase the effective output impedance of NFET **418**, thus making its performance more like that of an ideal current source.

Please replace paragraph [0027] on page 11 with the following amended paragraph.

[0027] Three main branches of current paths exist from the output **411** of PFET **410**, the current source (Isrc). A first current path (current sink path) exists to the current sink through PFET **412**, PFET **414**, NFET **416**, and NFET **418**. A second current path (gate current path) that passes charge to the gate of the pull-down driver transistor **404**

that passes through PFET **412**, PFET **414**, and to the gate of pull-down transistor **404**. The third current path exists for feedback (feedback current path) current through PFET **409**, PFET **413**, NFET **420**, feedback capacitor C 1, and the source to the drain of pull-down transistor **404**. The amount of current entering current node **411**, for example two units of current, equals the total current leaving current node **411** through the three main branches of current paths. The folded cascode amplifier current steers $i_{SRC}$ through NFET **420** or PFET **412**, depending on the value of ~~$i_{CAP}$~~ $i_{CAP1}$.

Please replace paragraph [0029] on page 12 with the following amended paragraph.

[0029] When the voltage on node **424** crosses the threshold voltage of the driver transistor, pull-down NFET **404,** current begins to flow between pad **402** and ground through NFET 404. This starts a negative transition on pad **402**. As the voltage at pad **402** starts to decrease, ~~$i_{CAP}$~~ $i_{CAP2}$ begins to flow through capacitor C1. In an embodiment, the feedback current through capacitor C1 corresponds to equation (2). This current flow results in a lower voltage at SUM, consequently turning on NFET **420**. As soon as NFET **420** is on, SUM does not go much lower and approximately all of $i_{CAP1}$ conducts through NFET **420** and the current mirror pair **409 413**. NFET **420** and the current mirror pair **409 413** drain this current from node **411**, reducing the current going through PFET **412** to gate **424**. The current mirror pair **409 413** multiply the amount current diverted from node **411** in proportion to the current flowing through the feedback capacitor. In an embodiment, when the slope of the signal at pad **402** is sufficient that ~~$i_{CAP}$~~ $i_{CAP2}$ is one unit (i.e., slope = target slope), then NFET **420** is

conducting one unit, leaving only one unit to flow through PFET **412** into gate **424**. However, since NFETs **416, 418** sink one unit of current, no net current enters into gate **424**. The gate voltage on pull-down transistor **404** stabilizes, thus fixing the transition rate at output pad **402**.

Please replace paragraph [0030] on page 12 with the following amended paragraph.

[0030] If the slope of the signal at pad **402** exceeds the target slope, then ~~$i_{CAP}$~~ $i_{CAP2}$ is greater than one unit and the current through PFET **412** becomes less than one unit. This means that the net current flow into gate **424** is negative and the gate voltage on pull-down transistor **404** decreases, acting to reduce the transition slope at pad **402**. This current balancing continues until the voltage at pad **402** reaches ground. At this point, the slope is forced to be zero again. No $i_{CAP1}$ flows and all the current from PFET **410** goes to gate **424**. Gate **424** starts charging again and eventually reaches substantially the voltage of Vcc.